

Intel 4004

The **Intel 4004** is a 4-bit central processing unit (CPU) released by Intel Corporation in 1971. Sold for US\$60^[2], it was the first commercially produced microprocessor,^[3] and the first in a long line of Intel CPUs.

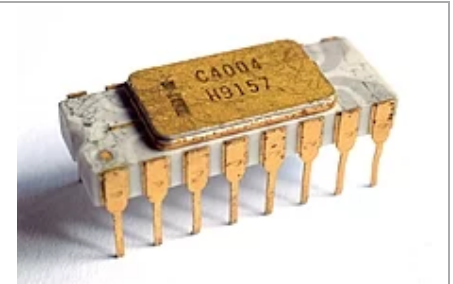
The chip design, implemented with the MOS silicon gate technology, started in April 1970, and was created by Federico Faggin who led the project from beginning to completion in 1971. Marcian Hoff formulated and led the architectural proposal in 1969, and Masatoshi Shima contributed to the architecture and later to the logic design. The first delivery of a fully operational 4004 occurred in March 1971 to Busicom Corp. of Japan for its 141-PF printing calculator engineering prototype (now displayed in the Computer History Museum in Mountain View, California).^[4] This calculator for which the 4004 was originally designed and built as a custom chip^[5] was first commercially available in July 1971.

Federico Faggin accomplished what no one had achieved before: to fit a general-purpose CPU into a small, commercial silicon chip. He invented how to design and layout 2300 random-logic transistors into a single chip with 5 times the speed and twice the circuit density (half the cost) of the incumbent metal gate technology. This unprecedented integration was achieved through the new process technology he invented at Fairchild Semiconductors in 1968, the MOS silicon gate technology (SGT), with which he also designed the first commercial IC (the Fairchild 3708). To design the Intel 4004, Faggin used the SGT with two new inventions of his, the "buried contact" and the "bootstrap load in silicon gate", which made possible the necessary speed, power, and cost for a useful general-purpose microprocessor.

The 4004 was the first random logic circuit integrated in one chip using the MOS (metal–oxide–semiconductor) silicon gate technology (SGT). It was the most advanced integrated circuit (IC) design undertaken up until then. Hoff, head of Intel's Application Research department, had formulated an architectural proposal consisting of a block architecture with an instruction set during 1969, while talking with Busicom engineers led by Shima and with the assistance of Stan Mazor. Hoff and Mazor were not MOS chip designers and did not participate in the actual design or development of the 4004.

The chip design was realized independently in the MOS department, different from Application Research. It could only be realized by a designer with deep knowledge of MOS process technology and of the new SGT. Faggin was hired at Intel in April 1970 from Fairchild Semiconductor to be the project leader and designer of the 4004 and he transferred to manufacturing a fully functional chip in March 1971. Faggin brought to Intel his mastery of the SGT that he had invented at Fairchild (in 1968) and used it to develop his novel methodology for

Intel 4004



White ceramic Intel C4004 microprocessor with grey traces

General information	
Launched	November 15, 1971
Discontinued	1981
Common manufacturer(s)	Intel
Performance	
Max. CPU clock rate	740-750 kHz
Data width	4 bits
Address width	12 bits (multiplexed)
Architecture and classification	
Application	Busicom calculator, arithmetic manipulation
Technology node	10 μm
Instruction set	4-bit BCD oriented
Physical specifications	
Transistors	2,250 ^[1]
Package(s)	16-pin DIP
Socket(s)	DIP16
History	
Successor	Intel 4040

random chip design that was key to making the first and all the early Intel microprocessors. Shima, representing Busicom, was engaged with Hoff and Mazor in the architectural phase during 1969 and he also assisted Faggin with the final logic design for 6 months in 1970.

In November 1971, with the prophetic advert "Announcing a new era in integrated electronics", the 4004 was made commercially available to the general market. The 4004 was the first monolithic processor, fully integrated in one small chip.^[6] Such a feat of integration was made possible by the use of the new silicon gate technology for integrated circuits, originally developed by Faggin (with Tom Klein) at Fairchild Semiconductor in 1968, which allowed twice the number of random-logic transistors and an increase in speed by a factor of five compared to the incumbent MOS aluminum gate technology.^[7] Faggin also invented the bootstrap load with silicon gate and the "buried contact", improving speed and circuit density compared with aluminum gate.^{[8][9][10][11][12]}

The 4004 microprocessor, the 4001 ROM, 4002 RAM, and 4003 Shift Register constituted the four chips in the Intel **MCS-4** chip set. With these components, small computers with varying amounts of memory and I/O facilities could be built.

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Contemporaneous CPU chips

Three other CPU chip designs were produced at about the same time: the Four-Phase Systems AL1, done in 1969; the MP944, completed in 1970 and used in the F-14 Tomcat fighter jet; and the Texas Instruments TMS-0100 chip, announced on 17 September 1971. The MP944 was a collection of six chips forming a single processor unit. The TMS0100 chip was presented as a "calculator on a chip" with the original designation TMS1802NC.^[13] This chip contains a very primitive CPU and can only be used to implement various simple four-function calculators. It is the precursor of the TMS1000, introduced in 1974, which is considered the first microcontroller—i.e., a computer on a chip containing not only the CPU, but also ROM, RAM, and I/O

functions.^[14] The MCS-4 family of four chips developed by Intel, of which the 4004 is the CPU or microprocessor, was far more versatile and powerful than the single-chip TMS1000, allowing the creation of a variety of small computers for various applications.

Zilog, the first company entirely dedicated to microprocessors and microcontrollers, was started by Federico Faggin and Ralph Ungermann at the end of 1974.

History and production



National Semiconductor was a second source manufacturer of the 4004, under their part number INS4004.^[15]

The first public mention of 4004 was an advertisement in the 15 November 1971 edition of *Electronic News*.^[16] The first delivery was to Busicom for their engineering prototype calculator in March 1971,^{[17][12]} followed by their 141-PF prototype calculator commercially available in the market in July 1971.^[18] Packaged in a 16-pin ceramic dual in-line package, the 4004 was the first commercially available computer processor designed and manufactured by chip maker Intel, which had previously made semiconductor memory chips. The chief designers of the chip were Federico Faggin, the leader of the project after the architectural definition was finalized with Busicom, who created the design methodology and the silicon-based chip design; Ted Hoff who formulated the architecture,^{[19][20]} both of Intel, and Masatoshi Shima of Busicom who assisted in the development.

Faggin, the sole chip designer among the engineers on the MCS-4 project, was the only one with experience in metal-oxide semiconductor (MOS) random logic and circuit design. He also had the crucial knowledge of the new silicon gate process technology with self-aligned gates, which he had created at Fairchild in 1968. At Fairchild in 1968, Faggin also designed and manufactured the world's first commercial IC using SGT, the Fairchild 3708^[21] that was featured on the cover of *Electronics* (29 September 1969).^[22] As soon as he joined the Intel MOS Department he created a new random logic design methodology based on silicon gate,^[18] and contributed many technology and circuit design inventions that enabled their single chip microprocessor to become a reality. His methodology set the design style for all the early Intel microprocessors and later for the Zilog Z80. He also led the MCS-4 project and was responsible for its successful outcome (1970–1971). Marcian "Ted" Hoff, head of the Application Research Department, contributed the architectural proposal for Busicom working with Stanley Mazor in 1969, then he moved on to other projects. When asked where he got the ideas for the architecture of the first microprocessor, Hoff related that Plessey, "a British tractor company",^[23] had donated a minicomputer to Stanford, and he had "played with it some" while he was there. Shima designed the Busicom calculator firmware and assisted Faggin during the first six months of the implementation. The manager of Intel's MOS Design Department was Leslie L. Vadász.^[24] At the time of the MCS-4 development, Vadász's attention was completely focused on the mainstream business of semiconductor memories and he left the leadership and the management of the MCS-4 project to Faggin.

Busicom had designed their own special-purpose LSI chipset for use in their Busicom 141-PF calculator with integrated printer. They based their design on the architecture of the Olivetti Programma 101, one of the world's first tabletop programmable calculators, which Olivetti introduced in 1965.^{[25][26][27]} Busicom commissioned Intel to develop their design for production. Like the Olivetti Programma 101, the Busicom design used serial read-write memory. The Busicom memory was based on MOS shift registers rather than the costly Olivetti memory based on magnetostriction wire.

Intel determined the Busicom design was too complex, since serial memories required more components, and would use 40 pins, a packaging standard different from Intel's own 16-pin standard. Intel proposed to develop a new design which could be produced with standard 16-pin DIP packaging, and would have a reduced instruction set.^[28] The memory simplification would come from using Intel's newly developed dynamic RAM memory. This new design was the 4004 chip, which is one of a set of four chips, along with

ROM, DRAM, and serial-to-parallel shift register chips. The 4004 was subsequently designed by Federico Faggin ^[29] using silicon gate technology and built of approximately 2,300 transistors^[1] and was followed the next year by the first ever 8-bit microprocessor, the 3,500 transistor 8008 (and the 4040, a revised and improved 4004). It was not until the development of the 40-pin 8080 in 1974, a project conceived and directed by Faggin ^[30] that the address and data buses would be separated, giving faster and simpler access to memory.

The 4004 employs a 10 µm process silicon-gate enhancement load pMOS technology on a 12 mm² die^[31] and can execute approximately 92,000 instructions per second; a single instruction cycle is 10.8 microseconds.^[32] The original clock rate design goal was 1 MHz, the same as the IBM 1620 Model I.

The Intel 4004 was designed by physically cutting sheets of Rubylith into thin strips to lay out the circuits to be printed, a process made obsolete by current computer graphic design capabilities.^[33]

For the purpose of testing the produced chips, Faggin developed a tester for silicon wafers of MCS-4 family that was itself driven by 4004 chip. The tester also served as a proof for the management that Intel 4004 microprocessor could be used not only in calculator-like products, but also for control applications.^[34]

Name and variants

When Faggin designed the MCS-4 family, he also christened the chips with distinct names: 4001, 4002, 4003, and 4004, breaking away from the numbering scheme used by Intel at that time which would have required the names 1302, 1105, 1507, and 1202 respectively. Had he followed Intel's number sequence, the idea that the chips were part of a family of components intended to work seamlessly together would have been lost.^[35] Intel's early numbering scheme for integrated circuits used a four-digit number for each component. The first digit indicated the process technology used, the second digit indicated the generic function, and the last two digits of the number were used to indicate the sequential number in the development of the component. The 8008 microprocessor was originally called 1201, per Intel's naming conventions. Before its market introduction, the 1201 was renamed 8008, following the new naming convention started with the 4001/4002/4003/4004.



The Unicom 141P is an OEM version of the Busicom 141-PF

Tadashi Sasaki attributes the basic invention to break the calculator into four parts with ROM (4001), RAM (4002), shift registers (4003) and CPU (4004) to an unnamed woman from the Nara Women's College present at a brainstorming meeting that was held in Japan prior to his first meeting with Robert Noyce from Intel, leading up to the Busicom deal.^[36]

The 4004 is part of the MCS-4 family of LSI chips that can be used to build digital computers with varying amounts of memory. The other members of the MCS-4 family are memories and input/output circuits, which are necessary to implement a complete computer. The 4001 is a ROM (read-only memory) with four lines of output; the 4002 is a RAM (random-access memory) with four lines of input/output. The 4003 is a static shift register to be used for expanding the I/O lines; e.g., for keyboard scanning or controlling a printer.

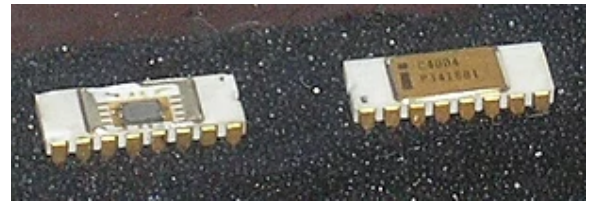
The 4004 includes functions for direct low-level control of memory chip selection and I/O, which are not normally handled by the microprocessor; however, its functionality is limited in that it cannot execute code from RAM and is limited to whatever instructions are provided in ROM (or an independently loaded RAM working as ROM—in either case, the processor is itself unable to write or transfer data into an executable memory space). The RAM and ROM parts were also unusual in their integration of output (and, in the

ROMs, input) ports that significantly reduced the minimum part count in an MCS-4 system, but required inclusion of a certain amount of processor-like logic on the chips themselves to accept, decode and execute relatively high-level data transfer instructions.

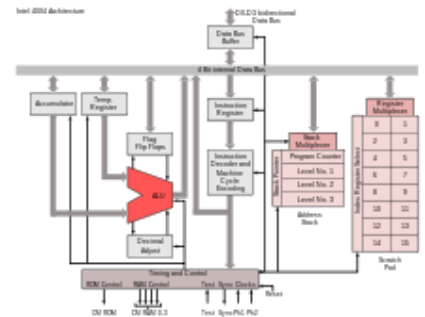
The standard arrangement for a 4004 system is anything up to 16×4001 ROM chips (in a single bank) and 16×4002 RAM chips (in four banks of four), which together provide the 4KB program storage, 1024 + 256 nibbles of data/status storage, plus 64 output and 64 input/output external data/control lines (which can themselves be used to operate, e.g. a 4003). Intel's MCS-4 documentation, however, claims that up to 48 ROM and RAM chips (providing up to 192 external control lines) "in any combination" can be connected to the 4004 "with simple gating hardware", but declines to give any further detail or examples of how this would actually be achieved.

Technical specifications

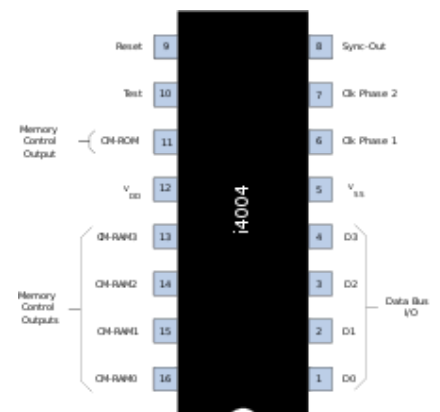
- Maximum clock rate is 740 kHz. The 4004 had this maximum clock rating upon its initial 1971 release^[Note 1]
- Instruction cycle time: minimum 10.8 μs ^[32] (8 clock cycles / machine cycle)
- Instruction execution time 1 or 2 machine cycles (10.8 or 21.6 μs), 46250 to 92500 instructions per second.
 - Adding two 8-digit numbers (32 bits each, assuming 4-bit BCD digits) takes a claimed 850 μs , or approximately 79 machine cycles (632 clock ticks), for an average of just under 10 cycles (80 ticks) per digit pair and an operating speed of 1176×8 -digit additions per second^[Note 2]
- Separate program and data storage. Contrary to Harvard architecture designs, however, which use separate buses, the 4004, with its need to keep pin count down, uses a single multiplexed 4-bit bus for transferring:
 - 12-bit addresses
 - 8-bit instructions
 - 4-bit data words
- Able to directly address 5120 bits (equivalent to 640 bytes) of RAM, stored as 1280 4-bit "characters" and organised into groups representing 1024 "data" and 256 "status" characters (512 and 128 bytes).^[Note 3]
- Able to directly address 32,768 bits of ROM, equivalent to and arranged as 4096 8-bit words (i.e. bytes).^[Note 4]
- Instruction set contained 46 instructions (of which 41 were 8 bits wide and 5 were 16 bits wide)
- Register set contains 16 registers of 4 bits each
- Internal subroutine stack, 3 levels deep.



Two C4004 DIPs with one opened to show the die.



Intel 4004 architectural block diagram



Intel 4004 DIP chip pinout

Logic levels

Intel 4004 registers

1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 (bit position)

Symbol	Min	Max	Unit
V _{SS-DD}	+15-5%	+15+5%	V
V _{IL}	V _{DD}	V _{SS} -5.5	V
V _{IH}	V _{SS} -1.5	V _{SS} +0.3	V
V _{OL}	V _{SS} -12	V _{SS} -6.5	V
V _{OH}	V _{SS} -0.5	V _{SS}	V

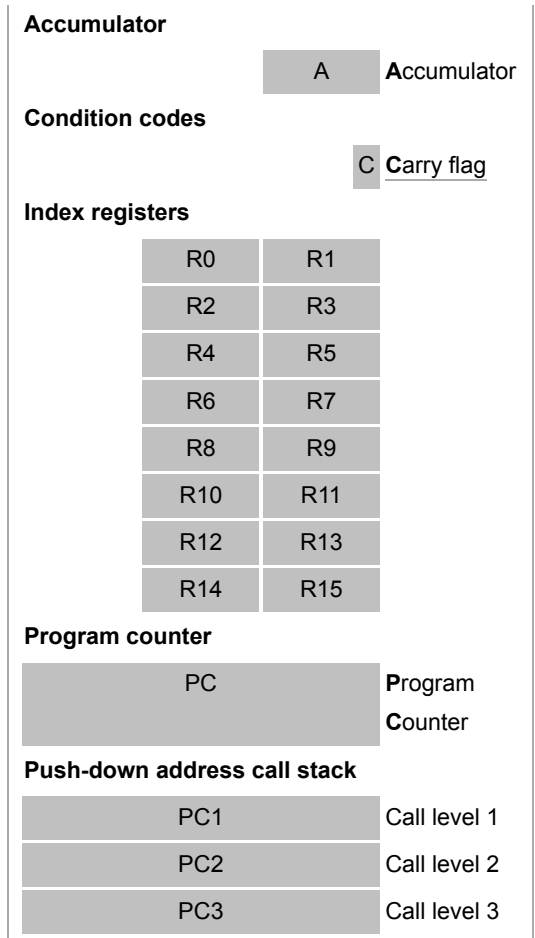
Support chips

- 4001: 256-byte ROM (256 8-bit *program* instructions), and one built-in 4-bit I/O port. A 4001 ROM+I/O chip cannot be used in a system along with a 4008/4009 pair.^[37]
- 4002: 40-byte RAM (80 4-bit *data* words), and one built-in 4-bit output port; the RAM portion of the chip is organized into four "registers" of 20 4-bit words:
 - 16 data words (used for mantissa digits in the original calculator design), accessed in a relatively standard manner, and
 - 4 status words (used for exponent digits and signs in the original calculator design), accessed using I/O type commands in place of the ROM's input channel
- 4003: 10-bit parallel output shift register for scanning keyboards, displays, printers, etc.
- 4008: 8-bit address latch for access to standard memory chips, and one built-in 4-bit chip select and I/O port
- 4009: program and I/O access converter to standard memory and I/O chips
- 4269: keyboard/display interface
- 4289: memory interface (combined functions of 4008 and 4009)

The minimum system specification described by Intel consists of a 4004 with a single 256-byte 4001 program ROM; there is no explicit need for separate RAM in minimal complexity applications thanks to the 4004's large number of onboard index registers, which represent the equivalent of 16×4 -bit or 8×8 -bit characters (or a mixture) of working RAM, nor for simple interface chips thanks to the ROM's built-in I/O lines. However, as project complexity increases, the various other support chips start to become useful.

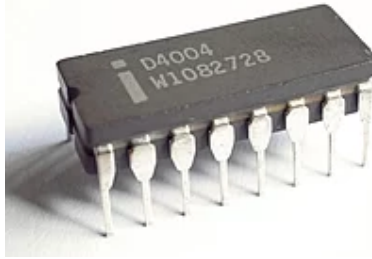
Packaging

Numerous versions of the Intel MCS-4 line of processors were produced. The earliest versions, marked C (like C4004), were ceramic and used a zebra pattern of white and gray on the back of the chips, often called "grey traces". The next generation of the chips was plain white ceramic (also marked C), and then dark grey ceramic (D). Many of the more recent versions of MCS-4 family were also produced with plastic (P).





The ceramic C4004 variant without grey traces.



The ceramic D4004 variant.



The plastic P4004 variant.

Use

The first commercial product to use a microprocessor was the Busicom calculator 141-PF. The 4004 was also used in the first microprocessor-controlled pinball game, a prototype produced by Dave Nutting Associates for Bally in 1974.

According to Nick Tredennick, a microprocessor designer and expert witness to the Boone/Hyatt patent case:

Here are my opinions from [the] study [I conducted for the patent case]. The first microprocessor in a commercial product was the Four Phase Systems AL1. The first commercially available (sold as a component) microprocessor was the 4004 from Intel.^[38]

A popular myth has it that Pioneer 10, the first spacecraft to leave the solar system, used an Intel 4004 microprocessor. According to Dr. Larry Lasher of Ames Research Center, the Pioneer team did evaluate the 4004, but decided it was too new at the time to include in any of the Pioneer projects. The myth was repeated by Federico Faggin himself in a lecture for the Computer History Museum in 2006.^[39]

Legacy and value

Federico Faggin signed the 4004 with his initials because he knew that his silicon gate design embodied "the essence of the microprocessor". A corner of the die reads "F.F."^[35]

On 15 November 2006, the 35th anniversary of the 4004, Intel celebrated by releasing the chip's schematics, mask works, and user manual.^[40] A fully functional 41×58 cm,^[41] 130× scale replica of the Intel 4004 was built using discrete transistors and put on display in 2006 at the Intel Museum in Santa Clara, California.^[42]

On 15 October 2010, Faggin, Hoff, and Mazor were awarded the National Medal of Technology and Innovation by President Barack Obama for their pioneering work on the 4004.^[43]



In the lower-right corner of the CPU are the initials "F.F."

See also

- Central Air Data Computer - first 20-bit military microprocessor was released in June 1970 for US Navy F-14 Tomcat fighter jet, about 1.5 years before the Intel 4004 was released

Notes

1. Although the early documentation states "0.75 MHz", this is at odds with the timing diagrams which specify a minimum overall cycle time of 1350 ns (=741 kHz) and a maximum of 2010 ns (=498 kHz)
2. This statistic comes from the same document as the "0.75 MHz" claim and which appears to inaccurately round off the true figures for the purposes of summary. 850 μ s with a minimum 10.8 μ s cycle time would in truth be 78.7 machine cycles, or roughly 629 clock ticks. As the processor is locked into an 8-tick cycle, it is more likely this operation would take 79 or even 80 full cycles, thus 632 to 640 ticks and 853 to 864 μ s (or 854 to 865 μ s at a true 740 kHz), and reducing the actual execution speed to 1157 ~ 1172 (or 1156 ~ 1171) 8-digit additions per second
3. However, this could only be used as working / data memory, and was non-executable: program code could not be stored in or run from RAM, as the processor kept the two memory areas strictly segregated at the microcode level. Instruction fetching forced assertion of the ROM chip-select line (and deassertion of the RAM select lines), and the chip had no way to "write" data to anything other than an IO port whilst the ROM area was selected.
4. The only part of the 4004 memory space capable of storing executable code, though also usable for general purpose storage

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- Cover and abstract of the IEDM (International Electron Devices Meeting) Program (October 1968) (http://www.intel4004.com/images/iedm_covart.jpg). The Silicon Gate Technology (SGT) was first presented by its developer, Federico Faggin, at the IEDM on 23 October 1968, in Washington, D.C. It was the only commercial process technology for the fabrication of MOS integrated circuits with self-aligned gate that was later universally adopted by the semiconductor industry. The SGT was the first technology to produce commercial dynamic RAMs, CCD image sensors, non volatile memories and the microprocessor, providing for the first time all the fundamental elements of a general purpose computer with LSI integrated circuits.
- Cover of Electronics Magazine (29 September 1969) (http://www.intel4004.com/images/elect_cov_pg1.jpg). The Electronics article introduces the Fairchild 3708, designed by Federico Faggin in 1968. It was the world's first commercial integrated circuit using the Silicon Gate Technology, proving its viability.
- Initials F.F. (Federico Faggin) on the 4004 design (1971) (<http://www.intel4004.com/sign.htm>). The 4004 bears the initials F.F. of its designer, Federico Faggin, etched on one corner of the chip. Signing the chip was a spontaneous gesture of proud authorship and was also an original idea imitated after him by many Intel designers.
- Busicom 141-PF Printing Calculator Engineering Prototype (1971) (<http://www.computerhistory.org/revolution/digital-logic/12/285/1534>). (Gift of Federico Faggin to the Computer History Museum, Mountain View, CA). The CHM collection catalog shows pictures of the engineering prototype of the Busicom 141-PF desktop calculator. The engineering prototype used the world's first microprocessor to have ever been produced. This one-of-a-kind prototype was a personal present by Busicom's president Mr. Yoshio Kojima to Federico Faggin for his successful leadership of the design and development of the 4004 and three other memory and I/O chips (the MCS-4 chipset). After keeping it in his home for 25 years, Faggin donated it to the CHM in 1996.

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Further reading

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- IEEE Solid State Circuits Magazine, Winter 2009 Vol.1 No.1. "The 4004 microprocessor of Faggin, Hoff, Mazor, and Shima". (<http://ieeexplore.ieee.org/xpl/tocresult.jsp?isYear=2009&isnumber=4776521&Submitt32=View+Contents>)
- The MOS Silicon Gate Technology and the First Microprocessors (http://www.intel4004.com/The_MOS_Silicon_Gate_Technology_and_the_First_Microprocessors.pdf), by Federico Faggin published in *La Rivista del Nuovo Cimento*, Italian Physical Society, Vol. 38, No. 12, 2015.
- "How we made the microprocessor" by Federico Faggin. *Nature Electronics*, Vol. 1, January 2018. Published online: 2018-01-08

External links

- Intel's First Microprocessor—the Intel 4004: Intel Museum (Intel Corporate Archives) entry (<http://www.intel.com/museum/archives/4004.htm>)
- The Intel 4004: A testimonial from Federico Faggin, designer of the 4004 and developer of its enabling technology (<http://www.intel4004.com/>)
- The New Methodology for Random Logic Design Used in the 4004 and in All the Early Intel Microprocessors (<http://www.intel4004.com/mrld.htm>)
- Interview with Masatoshi Shima (http://www.ieeeeghn.org/wiki/index.php/Oral-History:Masatoshi_Shima#LSI_for_Desktop_Calculators)
- MCS-4 Micro Computer Set Data Sheet (12 pp) (<http://smithsonianchips.si.edu/ice/4004thb.htm>)
- Intel 4004 -- 45th Anniversary Project (<http://www.4004.com>), Schematics at the unofficial 4004 website, and a simulator in Java. Fully functional 130x scale replicas of the 4004 built using discrete transistors.
- The Crucial Role of Silicon Design in the Invention of the Microprocessor (<http://www.intel4004.com/hyatt.htm>)
- High resolution light microscope pictures of an Intel 4004 die together with a basic explanation of CMOS logic (<https://web.archive.org/web/20110723120701/http://www.flylogic.net/blog/?p=63>)
- Intel 4004 Emulator, Assembler, and Disassembler: Simple programming tools for Intel 4004 in Javascript (<http://www.e4004.szyc.org/>)
- Datasheet Intel 4004 (<http://datasheets.chipdb.org/Intel/MCS-4/datashts/intel-4004.pdf>)
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- BuscomV2p1 schematic (<http://www.4004.com/assets/BuscomV2p1.jpg>)
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