

npm start

Not implemented yet.

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Roadmap

an HDL

Design the ASIC

Ethereum)

physical machines

Simulate the RTL design

Go to http://localhost:5000 in your web browser.

RTL Microarchitecture Simulator

Loading Microarchitecture

Implementation to FPGA

Understand the WebAssembly ISA

Implement the <u>mircoarchitecture</u> in

This will be a GUI simulator of the

This simulator will become the specification for

It will allow us to quickly experiment with

o It will allow us to iterate and learn how the

Implement the microarchitecture as an RTL design in

HTML/CSS/JavaScript

microarchitecture

the microarchitecture

hardware configurations

Test the implementation on an FPGA

Why is this a good idea?

Maybe it's not, but who cares

The world is moving to WebAssembly

target for low-level languages first

speeds on a variety of underlying ISAs

Some of the biggest and potentially most world-

• The bytecode is being designed as a compilation

• The bytecode is meant to execute at near-native

 Java processors already offer potential benefits, even being compilation targets for a high-level language

 Cutting out the translation from WebAssembly to the underlying ISAs could provide efficiency benefits

• We could get rid of WebAssembly virtual machines

entirely, and replace them with WebAssembly

changing projects are implementing their virtual

machines as WebAssembly virtual machines (DFINITY,

microarchitecture should work

 If <u>all SIM cards are Java processors</u>, imagine what WebAssembly processors could do. I'm betting that WebAssembly is a better bytecode than Java bytecode for what Java bytecode is doing with microcontrollers, so WebAssembly could take over all spaces that Java processors currently have

Prior art

- https://en.wikipedia.org/wiki/Jazelle
- https://stackoverflow.com/questions/1153076/does-android-castrate-the-arms-jazelle-technology
- https://en.wikipedia.org/wiki/Lisp_machine
- https://en.wikipedia.org/wiki/Java_processor
- https://en.wikipedia.org/wiki/Highlevel_language_computer_architecture

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